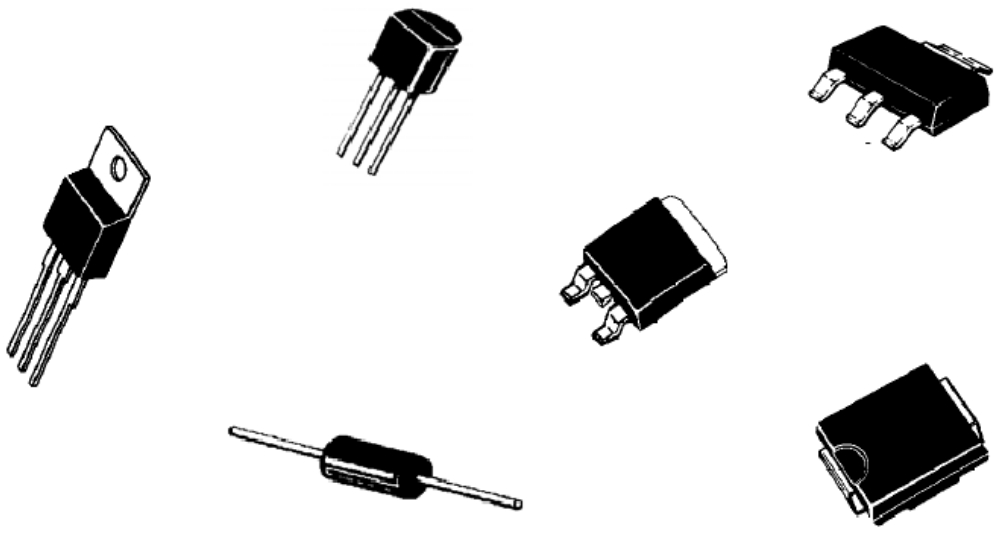
AEC - Q101 - Rev - D
May 18, 2013

# FAILURE MECHANISM BASED STRESS TEST QUALIFICATION FOR DISCRETE SEMICONDUCTORS IN AUTOMOTIVE APPLICATIONS



Automotive Electronics Council
Component Technical Committee

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## Attachments

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## Acknowledgment

Any document involving a complex technology brings together experience and skills from many sources. The Automotive Electronics Council would especially like to recognize the following significant contributors to the revision of this document:

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# FAILURE MECHANISM BASED STRESS TEST QUALIFICATION FOR DISCRETE SEMICONDUCTORS IN AUTOMOTIVE APPLICATIONS

***Text enhancements and differences made since the last revision of this document are shown as underlined areas. Several figures and tables have also been revised, but changes to these areas have not been underlined.***

***Unless otherwise stated herein, the date of implementation of this standard for new qualifications and re-qualifications is as of the publish date above.***

## 1. SCOPE

This document defines minimum stress test driven qualification requirements and references test conditions for qualification of discrete semiconductors (e.g. transistors, diodes, etc.). This document does not relieve the supplier of their responsibility to meet their own company's internal qualification program. Additionally, this document does not relieve the supplier from meeting any user requirements outside the scope of this document. In this document, "user" is defined as any company developing or using a discrete semiconductor part in production. The user is responsible to confirm and validate all qualification and assessment data that substantiates conformance to this document.

### 1.1 Purpose

The purpose of this specification is to determine that a part is capable of passing the specified stress tests and thus can be expected to give a certain level of quality / reliability in the application.

### 1.2 Reference Documents

Current revision of the referenced documents will be in effect at the date of agreement to the qualification plan. Subsequent qualification plans will automatically use updated revisions of these referenced documents.

#### 1.2.1 Military

MIL-STD-750 Test Methods for Semiconductor Devices

#### 1.2.2 Industrial

UL-STD-94 Test for Flammability of Plastic Materials of Parts in Devices and Appliances.
JEDEC JESD-22 Reliability Test Methods for Packaged Devices
J-STD-002 Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires.
J-STD-020 Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
JESD22-A113 Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
J-STD-035 Acoustic Microscopy for Nonhermetic Encapsulated Electronic Components

#### 1.2.3 Automotive

AEC-Q001 Guidelines for Part Average Testing
AEC-Q005 Pb-Free Test Requirements
AEC-Q101-001 ESD (Human Body Model)
AEC-Q101-003 Discrete Component Wirebond Shear Test

AEC-Q101-004 Miscellaneous Test Methods
- Unclamped Inductive Switching
- Dielectric Integrity
- Destructive Physical Analysis

AEC-Q101-005 ESD (Charged Device Model)
AEC-Q101-006 Short Circuit Reliability Characterization of Smart Power Devices for 12V Systems

#### 1.2.4 Other

QS-9000
ISO-TS-16949

#### 1.2.5 Decommissioned

AEC-Q101-002 ESD Machine Model
- Removed from JEDEC due to obsolescence. HBM and CDM cover virtually all known ESD-related failure mechanisms.

### 1.3 Definitions

#### 1.3.1 AEC Q101 Qualification

Successful completion and documentation of the test results from requirements outlined in this document allows the supplier to claim that the part is “AEC-Q101 qualified”. The supplier, in agreement with the user, can perform qualification at sample sizes and conditions less stringent than what this document requires. However, that part cannot be considered “AEC-Q101 qualified” until such time that the unfulfilled requirements have been successfully completed. For ESD, it is highly recommended that the passing voltage be specified in the supplier datasheet with a footnote on any pin exceptions. This will allow suppliers to state, e.g., "AEC-Q101 qualified to ESD H1B", implying that supplier passes all AEC tests except the ESD level. Note that there are no "certifications" for AEC-Q101 qualification and there is no certification board run by AEC to qualify parts.

The minimum temperature range for discrete semiconductors per this specification shall be -40$^{o}$C to +125$^{o}$C operational, the minimum range for all LEDs shall be -40$^{o}$C to +85$^{o}$C operational. (Note: Some parts may be derated to zero at the maximum temperature.)

#### 1.3.2 Approval for Use in an Application

"Approval" is defined as user approval for use of a part in their application. The user’s method of approval is beyond the scope of this document.

#### 1.3.3 Terminology

In this document, “part” refers to the same entity as would “device” or “component”, that is, a singulated diode, transistor, varistor, etc. with the die molded in a plastic mold compound with metal leads for board attachment.

## 2. GENERAL REQUIREMENTS

### 2.1 Precedence of Requirements

In the event of conflict in the requirements of this specification and those of any other documents, the following order of precedence applies:

a. The purchase order
b. The individual agreed upon part specification
c. This document
d. The reference documents in Section 1.2 of this document
e. The supplier's data sheet

For the part to be considered qualified per this specification, the purchase order and/or individual part specification cannot waive or detract from the requirements of this document.

### 2.2 The Use of Generic Data to Satisfy Qualification and Re-qualification Requirements

The use of generic (family) data to simplify the qualification/re-qualification process is encouraged. To be considered, the generic data must be based on the following criteria:

a. Part qualification requirements listed in Table 2.
b. Matrix of specific requirements associated with each characteristic of the part and manufacturing process as shown in Table 3.
c. Definition of family guidelines established in Appendix 1.
d. Represent a random sample of the normal population.

Appendix 1 defines the criteria by which parts are grouped into a qualification family for the purpose of considering the data from all family members to be equal and generically acceptable to the qualification of the part in question.

With proper attention to these qualification family guidelines, information applicable to other parts in the family can be accumulated. This information can be used to demonstrate generic reliability of a part family and minimize the need for part-specific qualification test programs. This can be achieved through qualification of a range of parts representing the “four corners” of the qualification family (e.g., highest/lowest voltage, largest/smallest die, etc.). Sources of generic data should come from supplier-certified test labs, and can include internal supplier's qualifications, user-specific qualifications and supplier's in-process monitors. The generic data to be submitted must meet or exceed the test conditions specified in Table 2. Table 1 provides guidelines showing how the available part test data may be applied to reducing the number of lots required for qualification. Electrical characterization to the individual user part specification must be performed for each part submission, generic characterization data is not allowed. **The user(s) will be the final authority on the acceptance of generic data in lieu of specific part test data.**

### Table 1: Part Qualification/Re-qualification Lot Requirements

| Part Information | Lot Requirements for Qualification |
|---|---|
| New part, no applicable generic data. | Lot and sample size requirements per Table 2. |
| A part in a family is qualified. The part to be qualified is less complex and meets the Family Qualification Definition per Appendix 1. | Only part specific tests as defined in section 4.2 are required. Lot and sample size requirements per Table 2 for the required tests. |
| A new part that has some applicable generic data. | Review Appendix 1 to determine required tests from Table 2. Lot and sample sizes per Table 2 for the required tests. |
| Part process change. | Review Table 3 to determine which tests from Table 2 should be considered. Lot and sample sizes per Table 2 for the required tests. |

Table 2 defines a set of qualification tests that must be considered for both new part qualifications and re-qualification associated with a design or process change.

Table 3 defines a matrix of appropriate qualification tests that must be considered for any changes proposed for the part. Table 3 is the same for both new processes and requalification associated with a process change. This table is a superset of tests that the supplier and user should use as a baseline for discussion of tests that are required for the qualification/requalification in question. **It is the supplier's responsibility to present and document rationale for why any of the highlighted tests need not be performed.**

## 2.4 Test Samples

### 2.4.1 Lot Requirements

Lot requirements are designated in Table 2, herein.

### 2.4.2 Production Requirements

All qualification parts shall be produced on tooling and processes at the manufacturing site that will be used to support part deliveries at projected production volumes.

### 2.4.3 Reusability of Test Samples

Parts that have been used for nondestructive qualification tests may be used to populate other qualification tests. Parts that have been used for destructive qualification tests may not be used any further except for engineering analysis.

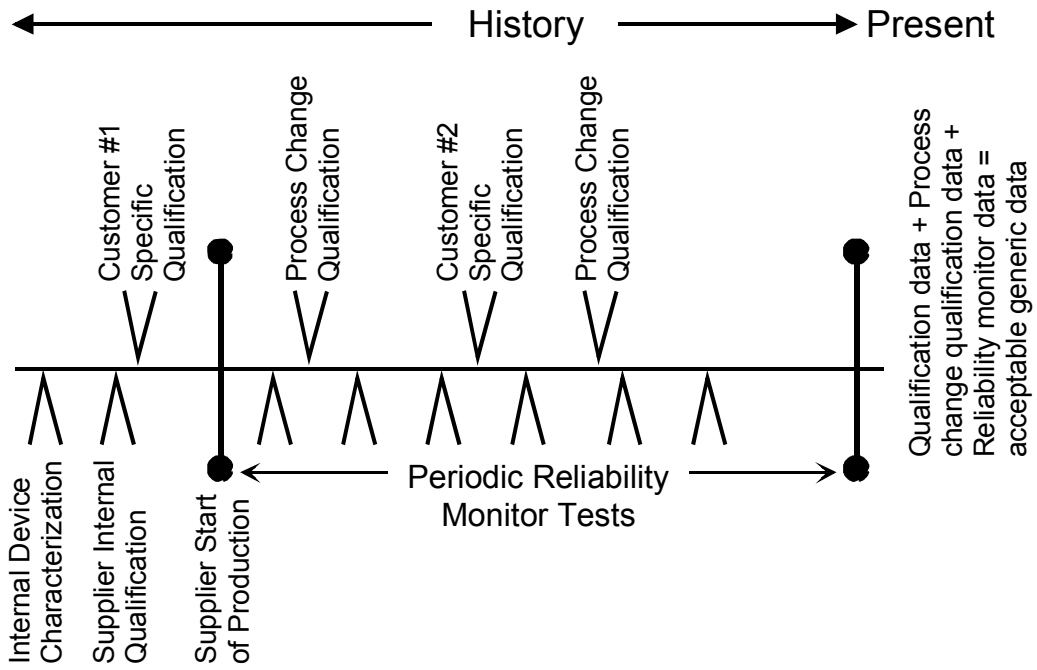
### 2.4.4 Sample Size Requirements

Sample sizes used for qualification testing and/or generic data submission must be consistent with the specified minimum sample sizes and acceptance criteria in Table 2. If the supplier elects to submit generic data for qualification/requalification, the specific test conditions and results must be reported. Existing applicable generic data should first be used to satisfy these requirements and those of Section 2.3 for each test requirement in Table 2. Part specific qualification testing should be performed if the generic data does not satisfy these requirements.

- The supplier must perform any combination of the specific part to be qualified and/or an acceptable generic part(s) that totals a minimum of 3 lots x 77 pcs/lot.

### 2.4.5 Time Limit for Acceptance of Generic Data

There are no time limits for the acceptability of generic data as long as the appropriate reliability data is submitted to the user for evaluation. Use the diagram below for appropriate sources of reliability data that can be used. This data must come from the specific part or a part in the same qualification family, as defined in Appendix 1. Potential sources of data could include any customer specific data (withhold customer name), process change qualification, and periodic reliability monitor data (see Figure 1).




**Note:** Some process changes (e.g., die shrink) will affect the use of generic data such that data obtained before these types of changes will not be acceptable for use as generic data.

**Figure 1: Generic Data Time Line**

### 2.4.6 Pre- and Post-Stress Test Requirements

All pre- and post-stress test parts must be tested to the electrical characteristics defined in the individual user part detail specification at room temperature.

### 2.5 Definition of Test Failure after Stressing

Test failures are defined as devices exhibiting any of the following criteria:

a. Parts not meeting the electrical test limits defined in the first user's part specification or appropriate supplier generic part specification. Minimum test parametric requirements shall be as specified in Appendix 5.

b. Parts not remaining within ± 20% of the initial reading of each test (with the exception of leakage limits which are not to exceed 10 times the initial value for moisture tests and 5 times the initial value for all others) after completion of environmental testing. Parts exceeding these guidelines must be justified by the supplier and approved by the user. For leakages below 100nA, tester accuracy may prevent a post stress analysis to initial reading.

c. Any part exhibiting external physical damage attributable to the environmental test.

If the cause of failure is agreed (by the manufacturer and the user) to be due to mishandling or ESD, the failure shall be discounted, but reported as part of the data submission.

### 2.6 Criteria for Passing Qualification/Re-qualification

Passing all appropriate qualification tests specified in Table 1, either by performing the tests (acceptance of zero failures using the specified minimum sample size) on the specific part or demonstrating acceptable family generic data (using the family definition guidelines defined in Appendix 1 and the total required lot and sample sizes), qualifies the part per this document.

Parts that have failed the acceptance criteria of tests required by this document require the supplier to satisfactorily determine root cause and corrective action to assure the user that the failure mechanism is understood and contained. The part shall not be considered as passing stress-test qualification until the root cause of the failure is determined and the corrective and preventive actions are confirmed to be effective. New samples or data may be requested to verify the corrective action. If generic data contains any failures, the data is not usable as generic data unless the supplier has documented corrective action or containment for the failure condition.

Any unique reliability tests or conditions requested by the user and not specified in this document shall be agreed upon between the supplier and user requesting the test, and will not preclude a device from passing stress-test qualification as defined by this document.

### 2.7 Alternative Testing Requirements

Any deviation from the test requirements and conditions listed in Table 2 are beyond the scope of this document. Deviations (e.g., accelerated test methods) must be demonstrated to the AEC for consideration and inclusion into future revisions of this document.

See Appendix 7: Guideline on Relationship of Robustness Validation to AEC-Q101 for more information.

## 3. QUALIFICATION AND REQUALIFICATION

### 3.1 Qualification of a New Part

Stress test requirements and corresponding test conditions for a new part qualification are listed in Table 2. For each qualification, the supplier must present data for ALL of these tests, whether it is stress test results on the specific part or acceptable generic family data. A review is to be made of

other parts in the same generic family to ensure that there are no common failure mechanisms in that family. Justification for the use of generic data, whenever it is used, must be demonstrated by the supplier and approved by the user. For each part qualification, the supplier must present Certificate of Design, Construction and Qualification to the requesting user. See Appendix 2.

### 3.2 Re-qualification of a Changed Part

Re-qualification of a part is required when the supplier makes a change to the product and/or process that impacts (or could potentially impact) the form, fit, function, quality and/or reliability of the part (see Table 3 for guidelines).

#### 3.2.1 Process Change Notification

The supplier will meet mutually agreed upon requirements for product/process changes.

#### 3.2.2 Changes Requiring Re-qualification

As a minimum, any change to the product, as defined above, requires performing the applicable tests listed in Table 2, using Table 3 to determine the re-qualification test plan. Table 3 should be used as a guide for determining which tests need to be performed or whether equivalent generic data can be submitted for the test(s).

#### 3.2.3 Criteria for Passing Re-qualification

All requalification failures shall be analyzed for root cause, with corrective and preventive actions established as required. The part and/or qualification family may be granted “qualification status” if, as a minimum, proper containment is demonstrated and approved by the user, until corrective and preventative actions are in place.

#### 3.2.4 User Approval

A change may not affect a part’s operating temperature grade, but may affect its performance in an application. Individual user authorization of a process change shall be based on a contract between Supplier and User, and is outside the scope of this document.

### 3.3 Qualification Test Plan

The supplier is requested to initiate a discussion with each user (as needed) resulting in completion of a signed Qualification Test Plan agreement as soon as possible after supplier selection for new parts, and at the time of notification (see Section 3.2.2) prior to process changes. The Qualification Test Plan, as defined in Appendix 3, shall be used to provide a consistent method of documentation supporting what testing will be performed as required by Tables 2 & 3.

## 4 QUALIFICATION TESTS

### 4.1 General Tests

Test details are given in Table 2. Not all tests apply to all parts. For example, certain tests apply only to hermetically packaged parts, others apply only to power MOSFET parts, and so on. The applicable tests for the particular part type are indicated in the "Note" column and the "Additional Requirements" column of Table 2. The "Additional Requirements" column of Table 2 also serves to highlight test requirements that supersede those described in the referenced test.

### 4.2 Part Specific Tests

The following tests must be performed on the specific part (i.e., family data is not allowed for these tests):

a. Electrostatic Discharge Characterization (Table 2, Test #11)

b. Parametric Verification (Table 2, Test #4) - The supplier must demonstrate that the part is capable of meeting parametric limits detailed in the individual user part specification.

### 4.3 Data Submittal Type

Data to be submitted to the user are classified in three types (Data Type column in Table 2):

#### 4.3.1 Data Type 1

Data (generic or specific) from these tests should be formatted as defined in Section 4.4 and included in each qualification submission.

#### 4.3.2 Data Type 2

Package specific data that should not be included with each qualification submission (except where the package is new). In place of this data the supplier can submit a "Document of Completion" that references successful completion of the specific test previously performed, provided no significant changes have been made. For Test #14 (Physical Dimensions), the Document of Completion should be completed referencing the appropriate user packaging specification.

#### 4.3.3 Data Type 3

Re-qualification data should be included in the qualification submission as required by Table 3. These tests shall be considered by the supplier during re-qualification plan development as useful tools to provide supporting rationale for new part qualification (including new packages) and/or process changes. It is the supplier's responsibility to present rationale for why any of these tests need not be performed.

### 4.4 Data Submission Format

A data summary shall be submitted as defined in Appendix 4. Raw data and histograms shall be submitted to the individual user upon request. **All data and documents (e.g., justification for non-performed tests, etc.) shall be maintained by the supplier in accordance with QS-9000 and/or TS-16949 requirements.**

### 4.5 Requirements for Testing Pb-free Components

The supplier shall follow the requirements of AEC-Q005 Pb-Free Test Requirements for all parts whose plating material on the leads/terminations contains <1000ppm by weight of lead (Pb).

| TABLE 2 - QUALIFICATION TEST DEFINITIONS | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| # | Stress | Abrv | Data Type | Note | Sample Size per Lot | # of Lots | Accept on # Failed | Reference (current revision) | Additional Requirements |
| 1 | Pre- and Post-Stress Electrical Test | TEST | 1 | NG | All qualification parts tested per the requirements of the appropriate part specification. | | 0 | User specification or supplier's standard specification | Test is performed as specified in the applicable stress reference at room temperature. |
| 2 | Pre-conditioning | PC | 1 | GS | SMD qualification parts before Test # 7, 8, 9, & 10. | | 0 | JESD22 A-113 | Performed on surface mount parts (SMDs) prior to Test # 7, 8, 9, & 10 only. TEST before and after PC. Any replacement of parts must be reported. |
| 3 | External Visual | EV | 1 | NG | All qualification parts submitted for testing | | 0 | JESD22 B-101 | Inspect part construction, marking and workmanship. |
| 4 | Parametric Verification | PV | 1 | N | 25 | 3 Note A | 0 | Individual AEC user specification | Test all parameters according to user specification over the part temperature range to insure specification compliance. |
| 5 | High Temperature Reverse Bias | HTRB | 1 | CDGK UVPX | 77 | 3 Note B | 0 | MIL-STD-750-1 M1038 Method A | 1000 hours at the maximum DC Reverse Voltage rated junction temperature specified in the user/supplier specification. The ambient temperature $T_A$ is to be adjusted to compensate for current leakage. TEST before and after HTRB as a minimum. (See note X HTRB.) **To be implemented on, or before, April 1, 2014.** |
| 5a | AC blocking voltage | ACBV | 1 | CDGU PY | 77 | 3 Note B | 0 | MIL-STD-750-1 M1040 Test condition A | 1000 hours at the maximum AC blocking voltage and junction temperature specified in the user/supplier specification. The ambient temperature $T_A$ is to be adjusted to compensate for current leakage. TEST before and after ACBV as a minimum. |
| 5b | High Temperature Forward Bias | HTFB | 1 | DGUZ | 77 | 3 Note B | 0 | JESD22 A-108 | 1000 hours at the maximum forward bias. TEST before and after HTFB as a minimum. |
| 5c | Steady State Operational | SSOP | 1 | CDGU O | 77 | 3 Note B | 0 | MIL-STD-750-1 M1038 Condition B (Zeners) | 1000 hours at rated IZ max, $T_A$ to rated $T_J$, TEST before and after SSOP as a minimum. |

| TABLE 2 - QUALIFICATION TEST DEFINITIONS (Continued) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| # | Stress | Abrv | Data Type | Note | Sample Size per Lot | # of Lots | Accept on # Failed | Reference (current revision) | Additional Requirements |
| 6 | High Temperature Gate Bias | HTGB | 1 | CDG MUP | 77 | 3 Note B | 0 | JESD22 A-108 | 1000 hours at the specified $T_J$(max) rating, with gate biased at 100% of maximum gate voltage rating indicated in the detail specification with part biased OFF. Can reduce duration to 500 hours through increasing $T_J$ by 25°C. TEST before and after HTGB as a minimum. |
| 7 | Temperature Cycling | TC | 1 | DGU | 77 | 3 Note B | 0 | JESD22 A-104 Appendix 6 | 1000 cycles ($T_A$ = minimum range of -55°C to maximum rated junction temperature, not to exceed 150°C). Can reduce duration to 400 cycles using $T_A$ (max) = 25°C over part maximum rated junction temperature or using $T_A$(max) = 175°C if the maximum rated junction temperature is above 150°C. TEST before and after TC. |
| 7a | Temperature Cycling Hot Test | TCHT | 1 | DGU1 | 77 | 3 Note B | 0 | JESD22 A-104 Appendix 6 | 125°C TEST after TC, followed by decap and wire pull on all wires from 5 devices per appendix 6 for parts with internal bond wire sizes 5 mil diameter and less. (Samples may be a sub set of test 7). **To be implemented on, or before, April 1, 2014.** |
| 7a alt | TC Delamination Test | TCDT | 1 | DGU1 | 77 | 3 Note B | 0 | JESD22 A-104 Appendix 6 J-STD-035 | 100% C-SAM inspection after TC, followed by decap, inspection or wire pull on all wires from 5 parts per appendix 6 for 5 highest delaminated parts. If C-SAM shows no delaminating, no decap, inspection and wire pull is required. **To be implemented on, or before, April 1, 2014.** |
| 7b | Wire Bond Integrity | WBI | 3 | DGUF | 5 | 3 Note B | 0 | MIL-STD-750 Method 2037 | 500 hours, $T_A$ = maximum rated Tj for bonding of dissimilar metals (e.g., Au/Al), decap and wire pull/bond inspection after WBI on all wires from a maximum of 5 parts. **To be implemented on, or before, April 1, 2014.** |
| 8 | Unbiased Highly Accelerated Stress Test | UHAST | 1 | CDG U | 77 | 3 Note B | 0 | JESD22 A-118 | 96 hours at TA=130°C/85%RH. TEST before and after 96 hours UHAST. |
| 8 alt | Autoclave | AC | 1 | CDG U | 77 | 3 Note B | 0 | JESD22 A-102 | 96 hours, TA = 121°C, RH = 100%, 15psig. TEST before and after AC. |

**TABLE 2 - QUALIFICATION TEST DEFINITIONS (Continued)**

| # | Stress | Abrv | Data Type | Note | Sample Size per Lot | # of Lots | Accept on # Failed | Reference (current revision) | Additional Requirements |
|---|---|---|---|---|---|---|---|---|---|
| 9 | Highly Accelerated Stress Test | HAST | 1 | CDG UV | 77 | 3 Note B | 0 | JESD22 A-110 | 96 hours at $T_A$=130°C/85%RH, or 264hrs TA=110°C /85%RH with part reverse bias at 80% of rated voltage up to a voltage above which arcing in the chamber will likely occur (typically 42V). TEST before and after HAST. |
| 9 alt | High Humidity High Temp. Reverse Bias | $H^3TRB$ | 1 | DGU V | 77 | 3 Note B | 0 | JESD22 A-101 | 1000 hours at $T_A$ = 85°C/85% RH with part reverse biased at 80% of rated breakdown voltage up to a maximum of 100V or limit of chamber. TEST before and after H3TRB as a minimum. |
| 9a | High Temperature High Humidity Bias | HTHHB | 1 | DGUZ | 77 | 3 Note B | 0 | JESD22 A-101 | 1000 hours at $T_A$ = 85°C/85% RH with part Forward biased. TEST before and after H3TRB as a minimum. |
| 10 | Intermittent Operational Life | IOL | 1 | DGTU WP | 77 | 3 Note B | 0 | MIL-STD-750 Method 1037 | Tested per duration indicated in Table 2A. $T_A$=25°C. Parts powered to insure $\Delta T_J \geq 100°C$ (not to exceed absolute maximum ratings). TEST before and after IOL as a minimum. |
| 10 alt | Power and Temperature Cycle | PTC | 1 | DGTU W | 77 | 3 Note B | 0 | JESD22 A-105 | Perform PTC if $\Delta T_J \geq 100°C$ cannot be achieved with IOL. Tested per duration indicated for Timing Requirements in Table 2A. Parts powered and chamber cycled to insure $\Delta T_J \geq 100°C$ (not to exceed absolute maximum ratings). TEST before and after PTC as a minimum. |
| 11 | ESD Characterization | ESD | 1 (HBM) 2 (CDM) | DW | 30 each HBM / CDM | 1 | 0 | AEC Q101-001, and Q101-005 | The supplier must document that the package could not hold sufficient charge to perform the test. TEST before and after ESD. |
| 12 | Destructive Physical Analysis | DPA | 1 | DG | 2 | 1 Note B | 0 | AEC-Q101-004 Section 4 | Random sample of parts that have successfully completed H3TRB or HAST, and TC. |
| 13 | Physical Dimension | PD | 2 | NG | 30 | 1 | 0 | JESD22 B-100 | Verify physical dimensions to the applicable user part packaging specification for dimensions and tolerances. |
| 14 | Terminal Strength | TS | 2 | DGL | 30 | 1 | 0 | MIL-STD-750 Method 2036 | Evaluate lead integrity of leaded parts only. |
| 15 | Resistance to Solvents | RTS | 2 | DG | 30 | 1 | 0 | JESD22 B-107 | Verify marking permanency. (Not required for laser etched parts or parts with no marking.) |

| TABLE 2 - QUALIFICATION TEST DEFINITIONS (Continued) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| # | Stress | Abrv | Data Type | Note | Sample Size per Lot | # of Lots | Accept on # Failed | Reference (current revision) | Additional Requirements |
| 16 | Constant Acceleration | CA | 2 | DGH (1) | 30 | 1 Note B | 0 | MIL-STD-750 Method 2006 | Y1 plane only, 15K g-force. TEST before and after CA. |
| 17 | Vibration Variable Frequency | VVF | 2 | DGH (2) | Items 16 through 19 are sequential tests for hermetic packages. (See note H on Legend page.) | | | JESD22 B-103 | Use a constant displacement of 0.06 inches (double amplitude) over the range of 20Hz to 100 Hz and a 50g constant peak acceleration over the range of 100 Hz to 2 KHz. TEST before and after VVF. |
| 18 | Mechanical Shock | MS | 2 | DGH (3) | | | 0 | JESD22 B-104 | 1500 g's for 0.5mS, 5 blows, 3 orientations. TEST before and after MS. |
| 19 | Hermeticity | HER | 2 | DGH (4) | | | 0 | JESD22 A-109 | Fine and Gross leak test per individual user specification. |
| 20 | Resistance to Solder Heat | RSH | 2 | DG | 30 | 1 | 0 | JESD22 A-111 (SMD) B-106 (PTH) | TEST before and after RSH. SMD parts shall be fully submerged during test and preconditioned per MSL rating. |
| 21 | Solderability | SD | 2 | DG | 10 | 1 Note B | 0 | J-STD-002 JESD22B102 | Magnification 50x. Reference solder conditions in Table 2B. Apply test method A for through-hole, or both test methods B and D for SMD. |
| 22 | Thermal Resistance | TR | 3 | DG | 10 each, pre- & post-change | 1 | 0 | JESD24-3, 24-4, 24-6 as appropriate | Measure TR to assure specification compliance and provide process change comparison data. |
| 23 | Wire Bond Strength | WBS | 3 | DGE | 10 bonds from min of 5 parts | 1 | 0 | MIL-STD-750 Method 2037 | Pre- & Post-process change comparison to evaluate process change robustness. |
| 24 | Bond Shear | BS | 3 | DGE | 10 bonds from min of 5 parts | 1 | 0 | AEC-Q101-003 | See attached procedure for details on acceptance criteria and how to perform the test. |
| 25 | Die Shear | DS | 3 | DG | 5 | 1 | 0 | MIL-STD-750 Method 2017 | Pre- & Post-process change comparison to evaluate process change robustness. |

| TABLE 2 - QUALIFICATION TEST DEFINITIONS (Continued) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| # | Stress | Abrv | Data Type | Note | Sample Size per Lot | # of Lots | Accept on # Failed | Reference (current revision) | Additional Requirements |
| 26 | Unclamped Inductive Switching | UIS | 3 | D | 5 | 1 | 0 | AEC-Q101-004 Section 2 | Pre- & Post-process change comparison to evaluate process change robustness (Power MOS and internally clamped IGBTs only). |
| 27 | Dielectric Integrity | DI | 3 | DM | 5 | 1 | 0 | AEC-Q101-004 Section 3 | Pre- & Post-process change comparison to evaluate process change robustness. All parts must exceed gate breakdown voltage minimum (Power MOS & IGBT only). |
| 28 | Short Circuit Reliability Characterization | SCR | 3 | DP | 10 | 3 Note B | 0 | AEC-Q101-006 | For smart power parts only. |
| 29 | Lead Free | LF | 3 | | - | - | - | AEC-Q005 | For all related solderability, solder heat resistance and whisker requirements. **To be implemented on, or before, April 1, 2014.** |

*** Note**: All electrical testing before and after the qualification stresses (including pre-conditioning) are performed to the limits detailed in the individual user specification at room temperature only. For generic qualifications, the supplier's standard specification limits at room temperature may be used.

## LEGEND FOR TABLE 2

Notes:

- A For parametric verification data, sometimes circumstances may necessitate the acceptance of only one lot by the user. Should a subsequent user decide to use a previous user's qualification approval, it will be the subsequent user's responsibility to verify an acceptable number of lots were used.
- B Where generic (family) data is provided in lieu of component specific data, 3 lots are required.
- C Not applicable for LED's, phototransistors, and other optical parts.
- D Destructive test, parts are not to be reused for qualification or production.
- E Ensure that each size wire is represented in the sample size.
- F For dissimilar metal bonding systems only (e.g., Au/Al).
- G Generic data allowed. See Section 2.3.
- H Required for hermetic packaged parts only. Items #16 through #19 are performed as a sequential test to evaluate mechanical integrity of packages containing internal cavities. Number in parentheses below notes indicates sequence.
- K Not applicable to voltage regulators (Zeners)
- L Required for leaded parts only.
- M Required for MOS & IGBT parts only.
- N Nondestructive test, parts can be used to populate other tests or they can be used for production.
- O Required for Voltage Regulators (Zeners) only.
- P Consideration should be made for whether this test is to be applied to a Smart Power part or substituted for a Q100 test. Elements for consideration include the amount of logic/sensing on the die, intended user application, switching speed, power dissipation, and pin count.
- S Required for surface mount parts only.
- T When testing diodes under Intermittent Op Life conditions the 100 degree junction temperature delta may not be achievable. Should this condition exist, a Power Temperature Cycling (Item 10alt) test shall be used in place of Intermittent Op Life (Item 10) to ensure the proper junction temperature changes occur. All other parts should use IOL.
- U For these tests only, it is acceptable to use unformed leaded packages (e.g., IPAK) to qualify new die going in the equivalent package (e.g., DPAK) provided the die size is within the range of sizes qualified for the equivalent package.
- V For bi-directional Transient Voltage Suppressor (TVS) devices, one-half the test duration in each direction shall be performed.
- W Not required for Transient Voltage Suppressor (TVS) parts. For TVS parts, PV data in Section 4.2 will be after 100% Peak Pulse Power (Pppm) has been performed to rated Ippm current.
- X For switching parts (e.g., fast/ultrafast rectifiers, Schottkys) the rated junction temperature specified in the user/supplier specifications refers to a switch mode application condition. For those parts that can experience thermal runaway in HTRB using a DC reverse condition on a switch mode part, the maximum rated junction temperature at the rated DC Reverse Voltage may not be specified in the user/supplier specification and those test conditions should be stated in the qualification test plan/report. Example: for a 100V Schottky part; 100V would be applied with $T_A$ adjusted to maximum $T_J$ capability without driving part into thermal runaway, Voltage, $T_A$ and $T_J$ achieved would be reported as test conditions in the qualification test plan/report.
- Y Required for Thyristors only.
- Z Required for LEDs only.
- 1 Required for MOSFETs parts with internal bond wire sizes 5 mil diameter and less.

## Table 2A: Timing Requirements for Intermittent Operational Life (Test #10) or Power Temperature Cycling (Test #10alt)

| Package Type | Number of Cycles Required $\Delta T_J \geq 100^oC$ | Number of Cycles Required $\Delta T_J \geq 125^oC$ | Time per cycle |
|---|---|---|---|
| All | 60,000/(x+y)<br>15,000 cycles | 30,000/(x+y)<br>7,500 cycles | Fastest capable (minimum 2 min. on/off) x min. on + y min. off |

Example 1: A package capable of 2 minutes on/4 minutes off would require 10,000 cycles [60,000/(2+4)] at $\Delta T_J \geq 100^oC$ or 5,000 cycles at $\Delta T_J \geq 125^oC$.
Example 2: A package capable of 1 minute on/1 minute off would require 15,000 cycles at $\Delta T_J \geq 100^oC$ or 7,500 cycles at $\Delta T_J \geq 125^oC$.
X = the minimum amount of time it takes for the part to reach the required $\Delta Tj$ from ambient temperature.
Y = the minimum amount of time it takes for the part to cool to ambient temperature from the required $\Delta Tj$.
The method of instrumentation, part mounting and heat sinking on the test board will influence x and y per package.

## Table 2B: Solderability Requirements (Test #21) for SnPb Plated Terminations

| Type | Test Method | Solder Temperature | Steam Age Category | Exception for Dry Heat |
|---|---|---|---|---|
| Leaded Through-Hole | A | 235°C | 3 | ---------- |
| SMD Standard Process | B | 235°C | 3 | ---------- |
| SMD Low Temperature Solder | B | 215°C | -- | 4hrs @ 155ºC (in lieu of steam age) |
| SMD Dissolution of Metals test | D | 260°C | 3 | ---------- |

*** Note:** Refer to AEC - Q005 Pb-Free Test Requirements for solderability requirements of Pb-free terminated parts.

# Automotive Electronics Council

**Component Technical Committee**

## Table 3: Process Change Guidelines for the Selection of Tests

**Note:** A letter or "●" indicates that performance of that stress test should be **considered** for the appropriate process change

| Table 2 Test # | 3 | 4 | 5/ abc | 6 | 7 | 7ab | 8/ alt | 9/ alt/a | 10/ alt | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Test Name / Change | External Visual | Parametric Verification | HTRB / ACBV / HTFB / SSOP | High Temp. Gate Bias | Temperature Cycle | TC Hot / TC Delam / WBI | UHAST / Autoclave | HAST / H$^3$TRB / HTHHB | IOL / PTC | ESD Characterization | Destruct. Phy. Analysis | Physical Dimensions | Terminal Strength | Resistance to Solvents | Constant Acceleration | Vibration | Mechanical Shock | Hermeticity | Resist. to Solder Heat | Solderability / AEC-Q005 | Thermal Resistance | Wire Bond Strength | Wire Bond Shear | Die Shear | Unclamp. Induct. Switch | Dielectric Integrity | Short Circuit Reliability Characterization | NOTES |
| **DESIGN** | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Wafer Thickness | | ● | ● | | ● | ● | | | ● | | ● | | | | | | | | x | | ● | ● | ● | | | | | F |
| Wafer Diameter | | ● | ● | ● | | | | | | | | | | | | | | | | | | | | | | | | |
| Die Size | | ● | ● | | ● | | | | ● | E | ● | | | | | | | | ● | | ● | | | ● | M | | ● | F |
| Layout | | ● | ● | ● | 3 | | | | ● | E | 3 | | | | | | | | | | | | | | M | | ● | |
| Field Termination | | ● | ● | | ● | | ● | ● | | E | ● | | | | | | | | | | | | | | M | | | |
| **WAFER FAB** | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Wafer Source | | ● | ● | | | | | ● | ● | | | | | | | | | | ● | | ● | | | | 9,M | | | R |
| Lithography | | ● | 4 | 4 | | | | 6,7 | | | | | | | | | | | | | | 1 | | | | | | P |
| Diffusion | | ● | 5,6 | 5 | | | 6 | 6 | | ● | 6 | | | | | | | | | | | | | | M | | | PR |
| Doping Profile/Schottky Barrier | | ● | 5,0 | | | | | | | ● | | | | | | | | | | | | | | | M | | | R |
| Ion Implantation | | ● | 5,6 | ● | | | 6 | 6 | | ● | 6 | | | | | | | | | | | | | | M | | | PR |
| Polysilicon | | ● | ● | ● | ● | | | | | E | ● | | | | | | | | | | | | | | M | ● | ● | P |
| Metallization (Top side) | | ● | 8 | | ● | ● | ● | ● | ● | E | ● | | | | | | | | ● | | | ● | ● | | | | ● | |
| Metallization (Back side) | | ● | | | ● | | | ● | ● | | | | | | | | | | ● | | ● | | | ● | | | | |
| Passivation/Glassivation | | ● | ● | ● | ● | | ● | ● | ● | ● | ● | | | | | | | | | | | ● | | | | | | |
| Oxide | | ● | | ● | 7 | | 6 | 6 | ● | E | 6,7 | | | | | | | | | | | | | | | ● | | |
| Epitaxic Growth | | ● | ● | | | | | | | | | | | | | | | | | | | | | | M | | | R |
| Etch | | ● | 6 | 4 | | | 6,7 | 6,7 | | | 6,7 | | | | | | | | | | | 1,7 | | | 8,M | 4 | | |
| Backside Operation | | ● | | | ● | | ● | ● | ● | | | | | | | | | | ● | | ● | | | ● | | | | A |
| Fab Site Transfer | | ● | ● | ● | ● | ● | ● | ● | ● | E | ● | | | | | | | | | | ● | ● | ● | ● | M | ● | | AIPRS |
| **ASSEMBLY** | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Die Overcoat | | | ● | ● | ● | | ● | ● | ● | | ● | | | | | | | H | | | | ● | | | | | | |
| Leadframe Plating/Lead Finish | D | | | | C | | C | C | | | | D | | D | | | | H | | D | C | 2C | | C | | | | |
| Leadframe Mat'l/Source | ● | | | | ● | ● | ● | ● | ● | | | ● | ● | | | | | H | ● | ● | ● | 2 | | ● | | | ● | AFX |
| Package/LF Dimension | | | | | ● | | | ● | ● | | | ● | | | | | | H | | | ● | | | ● | | | ● | |
| Wire Bonding | | ● | | | ● | ● | | ● | ● | | ● | | | | | | | | ● | | | ● | ● | | | | ● | |
| Die Scribe/Separation/Saw | | ● | | | ● | | | | ● | | | | | | | | | | | | | | | | | | | |
| Die Preparation/Clean | | ● | | | ● | | ● | ● | | | | | | | | | | | | | | ● | | ● | | | | X |
| Die Attach | | ● | | | ● | | ● | ● | ● | | | | | | | | | H | ● | | ● | | | ● | | | ● | AX |
| Encapsulation Material | ● | ● | ● | ● | ● | ● | ● | ● | ● | | ● | ● | | B | | | | H | ● | ● | ● | | | | | ● | | AFG |
| Encapsulation Process | ● | | ● | ● | ● | ● | ● | ● | ● | | ● | ● | | B | | | | H | ● | ● | | | | | | | | AG |
| Hermetic Sealing | H | | | | H | | H | H | | | H | | H | | H | H | H | H | H | | | | | | | | | |
| New Package | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | ● | B | H | H | H | H | ● | ● | ● | | | ● | | ● | ● | |
| Test Process/Sequence | | ● | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Package Marking | | | | | | | | | | | | | | B | | | | | | | | | | | | | | |
| Assembly Site Transfer | ● | ● | ● | ● | ● | ● | ● | ● | ● | | ● | ● | ● | ● | | | H | H | ● | ● | | ● | ● | ● | | | | AGISX |

A Acoustic Microscopy
B If not laser etched
C Only for Leadframe Plating change
D Only for Lead Finish change
E If Applicable
F Finite Element Analysis
G Glass Transition Temperature
H Hermetic part only
I Infant Mortality Rate
M Power MOS/IGBT parts only
P CV Plot (MOS only)
R Spreading Resistance Profile
S Steady State Mortality Rate
X X-Ray
1 If bond pads are affected
2 Verify #2 (package) post
3 Only for changes at the periphery
4 Only for oxide etches or etches prior to oxidation
5 For source or channel region changes
6 For field termination changes
7 For passivation changes
8 For contact changes
9 For epitaxial changes
0 Required for Schotthy Barrier changes

## Appendix 1: Definition of a Qualification Family

The qualification of a particular process will be defined within, but not limited to, the categories listed below. The supplier will provide a complete description of each process and material of significance. There must be valid and obvious links between the data and the subject of qualification.

For parts to be categorized in a qualification family, they all must share the same major process and materials elements as defined below. For each qualification test, two or more qualification families can be combined if the reasoning is technically sound (i.e., supported by rationale clearly detailing similarity). All parts using the same process and materials are to be categorized in the same qualification family for that process and are acceptable by association when one family member successfully completes qualification with the exception of the device specific requirements of Section 4.2.

Prior qualification data 3 years old or newer obtained from a part in a specific family may be extended to the qualification of subsequent parts in that family provided the supplier can insure no process changes have been made.

For broad changes that involve multiple attributes (e.g., site, material(s), process(es)), refer to Section 2.3 that allows for the selection of worst-case test vehicles to cover all the possible permutations.

### A1.1 Fab Process

Each process technology (e.g., Power MOS, Bipolar, Zener, etc.) must be considered and subjected to stress-test qualification separately. No matter how similar, processes from one fundamental fab technology cannot be used for the other.

Family requalification with the appropriate tests is required when the process or a material is changed. The important attributes defining a qualification family are listed below:

### A1.1.1 Wafer Fab Technology

- Power MOS
- Small Signal MOS
- Power Bipolar
- Small Signal Bipolar
- IGBT
- Optocoupler
- Phototransistors
- Rectifier
- Ultrafast Rectifier
- Schottky Rectifier
- Zener
- Transient Voltage Suppressor
- Pin
- Varactor
- Germanium
- Gallium Arsenide
- Photo Diodes
- SCRs
- LEDs

**A1.1.2 Wafer Fab Process** - consisting of the same attributes listed below:

- Process flow
- Layout design rules
- Number of masks
- Cell Density (where applicable)
- Lithographic process (e.g., contact vs. projection, E-beam vs. X-ray, photoresist polarity)
- Doping process (e.g., diffusion vs. ion implantation)
- Passivation/Glassivation material and thickness range
- Oxidation process and thickness range (for gate and field oxides)
- Front/back metallization material, thickness range and number of levels

**A1.1.3 Wafer Fab Site**

**A1.1.4 Example:**

3 lots of a FAB family in any package outline for the following Qualification tests:

- HTRB
- HTGB
- H3TRB / HAST

Example:
For a given FAB family of Gold doped Fast efficient rectifiers with a NiAu metal:

An axial-leaded 1A, 200V, 50mil$^2$ die size part
A surface mount 3A, 100V, 100mil$^2$ die size part
A through-hole TO-247, 30A, 600V, 135 mil$^2$ die size part

All 3 of these for the 3 tests above would constitute the requirement as 3 die sizes within the same FAB family under the same process controls.

**A1.2 Assembly Process**

The processes for each package type must be considered and subjected to stress-test qualification separately. For parts to be categorized in a qualification family, they all must share the same major process and material elements as defined below. Family requalification with the appropriate tests is required when the process or a material is changed. The supplier must submit technical justification to the user(s) to support the acceptance of generic data with package type, die sizes, paddle sizes and die aspect ratios different than the device being considered for stress-test qualification. The important attributes defining a qualification family are listed below:

**A1.2.1 Package Type** (e.g. TO-220, SOT-23, DO-41, SOIC, etc.)

- Range of paddle (flag) size qualified for the die size/aspect ratio under consideration.

**A1.2.2 Assembly Process** - consisting of the same attributes listed below:

- Leadframe base material
- Leadframe plating (internal and external to the package)
- Die attach material/method
- Wire bond material, wire diameter, and process
- Plastic mold compound or other encapsulation material

**A1.2.3 Assembly Site**

**A1.2.4 Example**

3 lots of a package family using any die structure that has the same die backside metallization will suffice for the following Qualification tests. It is highly desirable that two of the lots come from the maximum and minimum die size allowed by the package design rules.

- IOL / PTC
- TC
- AC / UHST
- H3TRB / HAST

**A1.3 Qualification of Multiple Families and Sites**

When the specific product or process attribute to be qualified or re-qualified (i.e., via process, material or site change) will affect more than one wafer fab family or assembly family, the qualification test vehicles should be three lots of a single part type from each of the technology and package families that are projected to be most sensitive to the changed attribute with sample sizes split to include a minimum of 30 pieces from each of 3 assembly lots from each assembly / fab site.

Below is the recommended process for qualifying changes across many process and product families:

a. Identify all products affected by the proposed process changes.

b. Identify the critical structures and interfaces potentially affected by the proposed change.

c. Identify and list the potential failure mechanisms and associated failure modes for the critical structures and interfaces. Conduct a risk assessment into potential failure mechanisms. Note that steps (a) to (c) are equivalent to the creation of an FMEA.

d. Define the product groupings or families based upon similar characteristics as they relate to the technology process and package families and device sensitivities to be evaluated, and provide technical justification to document the rationale for these groupings.

e. Provide the qualification test plan, including a description of the change, the matrix of tests and the representative products, which will address each of the potential failure mechanisms and associated failure modes.

f. Robust process capability must be demonstrated at each site (e.g., control of each process step, capability of each piece of equipment involved in the process, equivalence of the process step-by-step across all affected sites) for each of the affected process step(s).

## Appendix 2: Certification of Design, Construction and Qualification

**Supplier Name:** **Date:**

The following information is required to identify a part that has met the requirements of AEC-Q101. Submission of the required data in the format shown below is optional. **All entries must be completed; if a particular item does not apply, enter "Not Applicable".** This template can be downloaded from the AEC website at http://www.aecouncil.com.

**This template is available as a stand-alone document.**

| Item Name | Supplier Response |
|---|---|
| 1. User's Part Number: | |
| 2. Supplier Part Number/Generic Part Number: | |
| 3. Device Description: | |
| 4. Wafer/Die Fab Location & Process ID:<br>a. Facility name/plant #:<br>b. Street address:<br>c. Country: | |
| 5. Wafer Probe Location:<br>a. Facility name/plant #:<br>b. Street address:<br>c. Country: | |
| 6. Assembly Location & Process ID:<br>a. Facility name/plant #:<br>b. Street address:<br>c. Country: | |
| 7. Final Quality Control A (Test) Location:<br>a. Facility name/plant #:<br>b. Street address:<br>c. Country: | |
| 8. Wafer/Die:<br>a. Wafer size:<br>b. Die family:<br>c. Die mask set revision & name: | |
| 9. Wafer/Die Technology Description:<br>a. Wafer/Die process technology:<br>b. Gate oxide thickness (MOSFETs only):<br>c. Number of mask steps: | |
| 10. Die Dimensions:<br>a. Die width:<br>b. Die length:<br>c. Die thickness (finished): | |
| 11. Die (frontside) Metallization:<br>a. Die metallization material(s):<br>b. Number of layers:<br>c. Thickness (per layer):<br>d. % of alloys (if present): | |
| 12. Die Passivation:<br>a. Number of passivation layers:<br>b. Die passivation material(s):<br>c. Thickness(es) & tolerances: | |

| | |
|---|---|
| 13. Die Overcoat Material (e.g., Polyimide): | |
| 14. Die Prep Backside:<br>a. Die prep method:<br>b. Die metallization:<br>c. Thickness(es) & tolerances: | |
| 15. Die Separation Method:<br>a. Kerf width (μm):<br>b. Kerf depth (if not 100% saw):<br>c. Saw method: | Single ☐ Dual ☐ |
| 16. Die Attach:<br>a. Die attach material ID:<br>b. Die attach method:<br>c. Die placement diagram: | See attached ☐ Not available ☐ |
| 17. Package:<br>a. Type of package (e.g., plastic, ceramic, unpackaged):<br>b. JEDEC designation (e.g., MS029, MS034, etc.): | |
| 18. Mold Compound:<br>a. Mold compound supplier & ID:<br>b. Mold compound type:<br>c. Flammability rating:<br>d. Fire Retardant type/composition:<br>e. Tg (glass transition temperature)(°C):<br>f. CTE (above & below Tg)(ppm/°C): | UL 94 V1 ☐ UL 94 V0 ☐<br><br>CTE1 (below Tg) = _____ CTE2 (above Tg) = _____ |
| 19. Wire Bond:<br>a. Wire bond material:<br>b. Wire bond diameter (mils):<br>c. Type of wire bond at die:<br>d. Type of wire bond at leadframe:<br>e. Number of bonds over active area: | |
| 20. Leadframe (if applicable):<br>a. Header material:<br>b. Header width (mils):<br>c. Header length (mils):<br>d. Header plating composition:<br>e. Header plating thickness (μinch):<br>f. Leadframe material:<br>g. Leadframe bonding plating composition:<br>h. Leadframe bonding plating thickness (μinch):<br>i. External lead plating composition:<br>j. External lead plating thickness (μinch): | |
| 21. Thermal Resistance:<br>a. $\theta_{JA}$ °C/W (approx):<br>b. $\theta_{JC}$ °C/W (approx):<br>c. $\theta_{JL}$ junction-to-lead °C/W (approx):<br>d. $\theta_{JM}$ junction-to-mounting base °C/W (approx): | |

| | |
|---|---|
| 22. Maximum Process Exposure Conditions:<br><br>a. MSL @ rated SnPb temperature:<br>b. MSL @ rated Pb-free temperature: | ** Note: Temperatures are as measured on the center of the plastic package body top surface.*<br>_____ at _____ °C (SnPb)<br>_____ at _____ °C (Pb-free) |

| Attachments: | | Requirements: |
|---|---|---|
| Die Photo | ☐ | 1. A separate Certification of Design, Construction & Qualification must be submitted for each part number, wafer fab, and assembly location. |
| Package Outline Drawing | ☐ | |
| Die Cross-Section Photo/Drawing | ☐ | |
| Wire Bonding Diagram | ☐ | 2. Design, Construction & Qualification shall be signed by the responsible individual at the supplier who can verify the above information is accurate and complete. Type name and sign below. |
| Die Placement Diagram | ☐ | |

| | |
|---|---|
| Completed by: Date: | Certified by: Date: |
| Typed or Printed:<br><br>Signature:<br><br>Title: | |

## Appendix 3: Qualification Test Plan

The supplier is requested to complete and submit the Discrete Semiconductor Qualification Test Plan as part of the pre-launch Control Plan whenever qualification submission is required. Acceptance and subsequent sign-off of the plan will establish a qualification agreement between the user and the supplier determining requirements for both new parts and process changes prior to commencement of testing. Where "family" data is being proposed, the plan will document how the reliability testing previously completed fulfills the requirements outlined in this specification. An approved copy of the Qualification Test Plan shall be included with each qualification submission.

The test plan section of the form should detail ONLY the testing that will be performed on the specific part shown. For process change qualifications, multiple parts can be included on the same plan. Supporting generic or family data reports should be noted in the comment section and attached. When requesting use of generic or family data, attach a separate page detailing similarities or differences between parts referencing the criteria in Appendix 1. There must be valid and obvious links between the data and the subject of qualification.

The example below is provided to demonstrate how the Qualification Test Plan Form, found on the AEC website, should be used. In this case, a bipolar discrete part was chosen as being representative of a typical new part qualification requesting reduced component testing by including generic test data. The part comes from a supplier who previously qualified the package, assembly site etc. This example is shown for illustration purposes only and should not limit any requirements from Table 1 herein.

| Page 1 of 1 | | Discrete Semiconductor Component Qualification Plan | | | | | | Rev: A 4/24/04 |
|---|---|---|---|---|---|---|---|---|
| User P/N: | N611045BFDAARA | User Component Engineer: | John Doe | | | | | |
| User Spec. #: | ES-N611045BFDAARA | General Specification: | AEC-Q101 | | | | | |
| Supplier: | Sam's Discount Semiconductors (SDS) | Supplier Manufacturing Site: | Shanghai, China | | | | | |
| Supplier Generic P/N: | PZT3904 | Required PPAP Submission Date: | 7/1/2004 | | | | | |
| Supplier Internal P/N: | SDF-3417-AR | Family Type: | Bipolar SOT-223, 20 mil square die | | | | | |
| Reason for Qual: | New device qualification | | | | | | | |

| Item | Test | Test Conditions | Exceptions | Est. Start | Est. Comp. | # Lots | S. S. | Remarks |
|---|---|---|---|---|---|---|---|---|
| 1 | TEST | Electrical Characterization @ 25C | | 4/1/2004 | 4/5/2004 | all | all | |
| 2 | Preconditioning | per AEC-Q101 | | 4/8/2004 | 4/10/2004 | all | all | |
| 3 | External Visual | per AEC-Q101 | | 4/11/2004 | 4/12/2004 | all | all | |
| 4 | Parametric Verification | Characterization @ -55, 25, & 150C | | 4/15/2004 | 4/19/2004 | 3 | 30 | |
| 5 | HTRB | Reverse biased @ 64V | | 4/22/2004 | 6/24/2004 | 3 | 77 | |
| 6 | HTGB | | N/A Bipolar device | | | | | |
| 7 | Temperature Cycling | | Use attached generic data for this package related test. | | | | | generic data uses -65/150C (rather than -55C) |
| 8 | Autoclave | Ta = 121C, P = 15PSIG, RH = 100% | Use attached generic data for this package related test. | | | | | |
| 9 | H3TRB | Reverse biased @ 64V | | 4/22/2004 | 6/24/2004 | 3 | 77 | |
| 10 | IOL | | T on/off = 2 minutes, 15,000 cycles | 4/22/2004 | 6/24/2004 | 3 | 77 | SDS internal standard |
| 11 | ESD | per AEC-Q101 | | 4/22/2004 | 6/24/2004 | 1 | 30 | |
| 12 | DPA | per AEC-Q101 | | 6/24/2004 | 6/24/2004 | 3 | 2 | 2 ea from H3TRB and TC only. |

Comments:
1. Supplier requests 1 lot qualification of this device type in addition to attached rel reports fo similar parts to total 3 lots.
Rel Report #23-602 (PZT3906, the PNP compliment of this part) and #23-665 (PZTA62 NPN Darlington with larger 35 MIL die)
2. In addition, the die is qualified in SOT-23 version of this device, the SOT-223 package is qualified with larger (35 MIL) bipolar die (N611002BFDAARA & N611007BFDBARA).
3. Attached quarterly reliability results for 2002 & 2003 on generic PZT3904.
4. These devices all share the same wafer and assembly processes.
5. Tests 14-23 covered by annual SOT-223 packaging qual last approved 11/03.

| Prepared by (supplier): | | Approved by (User): |
|---|---|---|
| Typed/Printed | | Typed/Printed |
| Signature | | Signature |
| Title | | Title |

* Note: This plan is only an example and does not represent all the required tests in this document.

**Figure A3.1: Example of Discrete Semiconductor Qualification Test Plan**

## Appendix 4: Data Presentation Format

The supplier is required to complete and submit an Environmental Test Summary and Parametric Verification Summary with each Discrete Semiconductor PPAP submittal. Figure A4.1 is an example of a completed Environmental Test Summary. Figure A4.2 is an example of a completed Parametric Verification Summary. The format of both summaries shall be followed. Soft copies of the formats may be found on the AEC website or is available upon request. Other equivalent formats are acceptable if approved by the user.

| **Supplier**<br>Sam's Discount Semiconductors | | **User Part Number**<br>N611045BFDAARA | | | |
|---|---|---|---|---|---|
| **Name of Laboratory**<br>SDS Qual Lab | | **Part Description**<br>Bipolar SOT-223 Transistor | | | |
| **Test #** | **Test Description** | **Test Conditions** | **# Lots** | **# Tested** | **# Failed** |
| 2 | Preconditioning | Per Spec | 3 | 77 | 0 |
| 3 | External Visual | Per Spec | 3 | 381 | 0 |
| 5 | HTRB | Reverse Biased @ 64V; Tj = 150C | 3 | 77 | 0 |
| 9 | H3TRB | Reverse Biased @ 64V; 85C/85%RH | 3 | 77 | 0 |
| 10 | IOL | T on/off = 2 min, 15K Cycles | 1 | 77 | 0 |
| 11 | ESD | Per Spec | 1 | 30 | N/A |
| 12 | DPA | Per Spec | 3 | 2 | 0 |
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*** Note**: This listing of test results is only an example and does not represent all the tests in this document.

**Figure A4.1: Environmental Test Summary Example**

| Supplier | | | | User Part Number | | | | |
|---|---|---|---|---|---|---|---|---|
| Sam's Discount Semiconductors | | | | N611045BFDAARA | | | | |
| Lot Number | | | | Temperature | | | | |
| JB-117A (Test Lot 2) | | | | 25 Degrees C | | | | |
| Test Name | Unit | Spec LSL | Spec USL | MIN | MAX | MEAN | STD.DEV. | Cpk |
| $BV_{CEO}$ | V | 40 | - | 46.3 | 54.2 | 49.4 | 1.1 | 1.45 |
| $BV_{CBO}$ | V | 60 | - | 65.7 | 73.9 | 69.4 | 1.21 | 1.7 |
| $BV_{EBO}$ | V | 6 | - | 6.7 | 8.3 | 7.2 | 0.9 | 1.64 |
| $I_{BL}$ | nA | - | 50 | 0.15 | 37.2 | 24.2 | 0.2 | 10.2 |
| $I_{CEX}$ | nA | - | 50 | 0.02 | 12.3 | 8.7 | 0.45 | 9.8 |
| $h_{FE}1$ | -- | 40 | - | 45.6 | 93.2 | 72.3 | 6.7 | 1.8 |
| $h_{FE}2$ | -- | 70 | - | 71.7 | 114.2 | 96.2 | 5.2 | 2.01 |
| $h_{FE}3$ | -- | 100 | 300 | 103.2 | 294.4 | 187.3 | 19.1 | 2.7 |
| $h_{FE}4$ | -- | 60 | - | 78.7 | 114.3 | 98.7 | 3.7 | 1.95 |
| $h_{FE}5$ | -- | 30 | - | 37.2 | 46.2 | 41.2 | 0.9 | 2.7 |
| $V_{CESAT}1$ | V | - | 0.2 | 0.07 | 0.17 | 0.12 | 0.011 | 1.81 |
| $V_{CESAT}2$ | V | - | 0.3 | 0.16 | 0.25 | 0.21 | 0.01 | 1.41 |
| $V_{BESAT}1$ | V | 0.65 | 0.85 | 0.71 | 0.81 | 0.76 | 0.01 | 2 |
| $V_{BESAT}2$ | V | - | 0.95 | 0.56 | 0.86 | 0.63 | 0.015 | 3.7 |
| $f_T$ | MHz | 300 | - | 463 | 587 | 505 | 12 | 1.72 |
| $C_{OBO}$ | pF | - | 4 | 2.7 | 3.6 | 3.13 | 0.15 | 2.1 |
| $C_{IBO}$ | pF | - | 8 | 2.6 | 4.5 | 3.25 | 0.2 | 2.2 |
| $h_{IE}$ | Kohm | 1 | 10 | 2.3 | 4.6 | 3.7 | 0.2 | 1.8 |
| $h_{RE}$ | $10^{-4}$ | 0.5 | 8 | 0.79 | 1.57 | 1.23 | 0.13 | 1.83 |
| $h_{fe}$ | -- | 100 | 400 | 214 | 363 | 303 | 9 | 3.8 |

**Figure A4.2: Parametric Verification Summary Example**

## Appendix 5: Minimum Parametric Test Requirements

For Table 1 Test #1 (Pre- & Post-Stress Electrical Test), the following electrical parameters shall be used (as a minimum):

Transistors

| Bipolar | FET | IGBT |
|---|---|---|
| $BV_{CEX}$ | $BV_{DSS}$ | $BV_{CES}$ |
| $I_{CEX}$ | $I_{DSS}$ | $I_{CES}$ |
| $I_{EBX}$ or $I_{CBX}$ | $I_{GSS}$ | $I_{GES}$ |
| $V_{CE(SAT)}$ | $R_{DS(ON)}$ | $V_{CE(SAT)}$ |
| $h_{FE}$ | $G_{fs}$ (if specified) | $h_{FE}$ |
| | $V_{GS(th)}$ or $V_{GS(OFF)}$ | $V_{GE(th)}$ |

Diodes

$V_F$, $I_R$, $V_{BR}$ (Diodes)
$V_F$, $I_R$, $I_V$ (LEDs)
$V_Z$ or $V_{CLAMP}$ (Zeners)
$R_F$ (PIN Diode, if applicable)

Varactors

$I_R$, $C_T$

Opto Electronics

$V_F$, $I_R$, $V_{BR}$ (Diodes)
$V_F$, $I_R$, $I_V$ (LEDs)
$BV_{CEO}$, $I_{CEO}$, $V_{CE(SAT)}$ (Transistors)

# Appendix 6: Plastic Package Opening for Wire Bond Testing, and Inspection

## A6.1 Purpose

The purpose of this Appendix is to define a guideline for opening plastic packaged devices so that reliable wire pull or bond shear results will be obtained. This method is intended for use in opening plastic packaged devices to perform wire pull testing after temperature cycle testing or for bond shear testing.

## A6.2 Materials and Equipment

### A6.2.1 Etchants

Various chemical strippers and acids may be used to open the package dependent on your experience with these materials in removing plastic molding compounds. Red Fuming Nitric Acid has demonstrated that it can perform this function very well on novolac type epoxies, but other materials may be utilized if they have shown a low probability for damaging the bond pad material.

For some part designs (i.e., green compound molded), etching by red fuming Nitric acid and sulfuric acid will etch Al wire/Al pad in high temperature. The process will damage 5mil Al (including below 5mil).

Room temperature etchants should be used where possible.

### A6.2.2 Plasma Strippers

Various suitable plasma stripping equipment can be utilized to remove the plastic package material.

## A6.3 Plastic Package Opening Procedure for Wire Bond Testing

a. Using a suitable end mill type tool or dental drill, create a small impression just a little larger than the chip in the top of the plastic package. The depth of the impression should be as deep as practical without damaging the loop in the bond wires.

b. Using a suitable chemical etchant or plasma etcher, remove the plastic material from the surface of the die, exposing the die bond pad, the loop in the bond wire, and at least 75% of the bond wire length.

**Caution:** Do not expose the wire bond at the leadframe. These bonds are frequently made to a silver plated area and many chemical etchants will quickly degrade this bond making wire pull testing impossible.

*** Note:** For some part designs, especially for small packages, mounting the part may be required to ensure the structural integrity of the package during the package opening process and wire pull testing.

c. Using suitable magnification, inspect the bond pad areas on the chip to determine if the package removal process has significantly attacked the bond pad metallization. If a bond pad shows areas of missing metallization, the pad has been degraded and shall not be used for bond shear or wire pull testing. Bond pads that do not show attack can be used for wire bond testing.

## A6.4 Plastic Package Opening Procedure for Wire Bond Inspection after Temperature Cycling

a. Using a suitable chemical etchant or plasma etcher, remove the plastic material from the surface of the die, exposing the die bond pad, the loop in the bond wire, the bond wire length, and the wire bond at the leadframe.

**Caution:** Care must be taken when exposing leadframe wire bonds. These bonds are frequently made to a silver plated area and many chemical etchants will quickly degrade this bond making wire pull testing impossible.

*** Note:** For some part designs, especially for small packages, mounting the part may be required to ensure the structural integrity of the package during the package opening process and wire pull testing.

b. Using suitable magnification, inspect the bonds for damage from Temp cycle delamination.

# Appendix 7: Guidance on Relationship of Robustness Validation to AEC-Q101

## A7.1 Scope

A qualification method has recently been developed with the intent of addressing application specific operations. Called Robustness Validation, this method considers the specific environmental and operational application conditions and the customer lifetime requirements to calculate the minimum required set of qualification test conditions, durations and sample sizes. It also utilizes a reliability knowledge matrix that identifies likely failure mechanisms associated with the application and part specifics. When examined closely, most suppliers utilize most, if not all, of the basic tenets of Robustness Validation in their part qualification processes. The AEC qualification requirements are used as a baseline of test conditions and durations in the field of automotive electronics. It is intended to cover the majority of the application areas in terms of use time and loading.

The test conditions, durations and sampling may not be appropriate in case:

- Components in advanced technologies and or new materials are considered
- Application has a demanding loading profile
- Application has an extended lifetime requirement
- Application has a specific failure rate target over lifetime below the LTPD range

In case one or more of the above cases apply, Robustness Validation represents an approach to systematically prove the suitability of a component for a given application and its mission profile. A mission profile is the collection of relevant environmental and functional loads that a component will be exposed to during its use lifetime. The knowledge gained by applying this approach can lead to an improvement in the reliability margin between the component (specification) space and the application (condition) space when a specific component is used in a specific customer application. (The knowledge gained by applying this approach can lead to improvement of the component, application and its manufacturing process under consideration). Robustness Validation is a knowledge based approach that uses stress tests which are defined to address specific failure mechanisms using suitable test vehicles which may not necessarily be the component itself. These tests are used to determine the robustness margin, which is the difference between the use life time and the time of failure. This can be quantified as a Robustness Indicator Figure (RIF) which will be defined in Section A7.3.3.2. The intention of the method is to design robust products with a sufficient and known safety margin. A robust product is one that is capable of functioning correctly and not failing under varying application and product conditions.

## A7.1.1 Purpose

The basic considerations of the current environmental test conditions, durations and sample sizes in AEC-Q101 are given in the next Sections:

a. Section A7.2 discusses the sample sizes
b. Section A7.3.1 describes the concept of use life time and mission profile
c. Section A7.3.2 presents a flowchart to show the relation between RV and AEC
d. Section A7.4 shows the basic calculations of stress durations and comparison with AEC-Q101

## A7.1.2 References

**SAE J1879/ZVEI** Handbook for Robustness Validation of Semiconductor Devices in Automotive Applications
**JEDEC JEP122** Failure Mechanisms and Models for Semiconductor Devices

## A7.2 Sample Size

Regarding the sampling the following considerations have to be taken into account:

a. No fails in 231 parts (77parts from 3 lots) are applied as pass criteria for the major environmental stress tests. In relation to Early Life Failure rates, this represents an LTPD (Lot Tolerance Percent Defective) = 1, meaning a maximum of 0.4% failures at 60% confidence level.

b. This sample size is NOT sufficient or intended for process control or PPM evaluation. Much larger sample sizes would be needed, but are not possible in terms of costs and time to market.

c. Three lots are used as a minimal assurance of some process variation between lots. A monitoring process has to be installed to keep process variations under control.

d. Larger sample sizes (and greater confidence) can be obtained through the use of generic data for devices with the same technology.

e. Sample sizes are limited by part and test facility costs, qualification test duration, and limitations in batch size per test.

f. Test vehicles can be used to reduce sample sizes by achieving sufficient acceleration without introducing failure mechanisms that are not replicative at normal use conditions. In case of some Discrete Devices like MOSFETs, die-level mechanisms such as electro-migration and soft or hard breakdown of gate oxide can be studied in these devices themselves.

## A7.3 Base Considerations

### A7.3.1 Use Lifetime and Mission Profile

The use lifetime assumptions drawn here are seen to be a typical class of requirement from a given OEM or Tier-1 customer and necessarily apply to most vehicle locations.

- 15 year equivalent to 131,400 hours (8760 hours per year)
- 12,000 hours engine on-time (800 hours per year)
- 3000 hours engine off time { idle} (200 hours per year)
- 116,400 hours non-operating time (7760 hours per year)
- 360,000 miles / 600,000 km (30 mph / 50 km/h)
- 54,750 engine on-off cycles (10 on-off cycles per day)

The mission profile itself is generated by adding information on thermal, electrical, mechanical and any other loading under use conditions, to the above lifetime requirements. A flowchart to show the relation between RV and AEC based on an assessment of the mission profile is discussed in Section A7.3.2.

### A7.3.2 Flow chart to validate the applicability of AEC-Q101

Two flow charts are available to facilitate both Tier-1 and Component Manufacturing in determining the applicability of AEC-Q101:

a. Flow Chart 1 in Figure A7.1 - describes the process at Component Manufacturer to assess whether a new component can be qualified by AEC-Q101.

b. Flow Chart 2 in Figure A7.2 - describes (1) the process at Tier 1 to assess whether a certain electronic component fulfills the requirements of the mission profile of a new Electronic Control Unit (ECU); and (2) the process at Component Manufacturer to assess whether an existing component qualified according to AEC-Q101 can be used in a new application.

The robustness margin is the key criterion. In addition, not shown in the flow chart, the expected end of life failure rate may be an important criterion.

Using the result of 0/231, an estimate can be given of the maximum intrinsic failure rate during useful life: e.g., 15 FIT based on Arrhenius Equation (with Ea = 0.7 eV and 55°C use vs. 150°C test) at 60% confidence level using the chi-square distribution ($\chi^2$), which relates observed and expected frequencies of an event.

### A7.3.3 Detailed Description of Flow Charts

#### A7.3.3.1 Basic Assessment and/or Assessment at ECU Level

A detailed description of flow chart steps is given below (numbers refer to these specific flow chart steps).

##### A7.3.3.1.1 Flow Chart Step 1.1: Determine Mission Profile

Items to consider in constructing a Mission Profile Assessment:

- Type of application
- Requirements of service life and usage
- Environmental conditions / Mounting location
- Construction of the ECU
- Power Dissipation of ECU and components
- Reliability requirements in terms of lifetime and related failure rates

A structured analysis of the mission profile will identify potential reliability risks in an early stage of development cycle, so that these risks can be addressed by appropriate component selection and validation.

##### A7.3.3.1.2 Flow Chart Step 1.2: Determine Mission Profile of the Component

Translation of ECU Mission Profile to component mission profiles, taking different loading on component level into account:

- Thermal: The thermal loading of the component is a combination of power dissipation in the component and thermal housekeeping of the ECU, and therefore influenced by design of component and ECU.

- Thermo-Mechanical: The thermo-mechanical loading of the component can be more or less severe compared to the thermo-mechanical loading of the ECU depending on ECU construction and PCB layout.

- Humidity: The moisture loading of the component can induce higher fail rates due to moisture diffusing its way to the die surface. The moisture at the die surface is not necessarily the same concentration as the moisture in the ambient environment due to the bias conditions used.

**A7.3.3.1.3 Flow Chart Step 1.3: Basic Calculation**

Performance of "basic calculation" facilitates the mission profile assessment via a high level check of the suitability of a component (or list of components) for the given application. These calculations enable the translation from the component mission profile to equivalent qualification test duration under specified conditions. The main considerations to decide on using the "basic calculation" are:

- Component is not developed and produced within a new technology.
- Operation of the component is not at the extreme of its specification.
- The component is not used in an unusual or unintended operation mode.

**A7.3.3.1.4 Flow Chart Step 1.4: Calculate Test Duration with Standard Acceleration Models**

By applying the "basic calculation", the mission profile is translated into an equivalent stress with the same conditions as the qualification standard test. Commonly accepted acceleration models and parameters are used and can be taken from the literature and/or standards (e.g., JEP122). This is explained in Section A7.4.

**A7.3.3.1.5 Flow Chart Step 1.5: Compare Calculation with AEC-Q101**

The calculated stress duration $t_{CALC}$ (in hrs or number of cycles) has to be compared with the standard qualification duration $t_{STAND}$.

**A7.3.3.1.6 Flow Chart Step 1.6: Critical/Marginal Determination**

In case $t_{STAND} > t_{CALC}$, the component is assumed to be not critical/marginal. The robustness margin is larger when the difference $t_{STAND} > t_{CALC}$ is larger. To express the robustness margin, the Robustness Indication Figure (RIF) can be used, which is in this case defined as the ratio between $t_{CALC}$ and $t_{STAND}$ : $RIF = t_{STAND} / t_{CALC}$.

**A7.3.3.1.7 Flow Chart 1 (Reliability Test Criteria for New Component), Result A: Perform Qualification According to AEC-Q101**

The robustness margin is not critical/ marginal (i.e., $t_{STAND} > t_{CALC}$), new component qualification can be performed according to AEC-Q101 test conditions.

**A7.3.3.1.8 Flow Chart 2 (Assessment of Existing, Qualified Component), Result A: AEC-Q101 Test Conditions Sufficient/Exceeded**

If the robustness margin is not critical/ marginal (i.e., $t_{STAND} > t_{CALC}$), the existing component qualified to AEC-Q101 test conditions meets or exceeds the new application requirements.

**A7.3.3.2 Mission Profile Validation on Component Level**

A detailed description of flow chart steps is given below (numbers refer to these specific flow chart steps).

**A7.3.3.2.1 Flow Chart Step 2.1: Determine Critical Failure Mechanisms**

The recommended base for assessing the critical failure mechanism(s) is the Robustness Validation Knowledge Matrix or JEP122. In this risk assessment the following considerations are important:

- New materials or interfaces
- New design or production techniques
- Critical use conditions

**A7.3.3.2.2 Flow Chart Step 2.2: Determine Acceleration Models**

In case acceleration models are in use in the company or known from the literature, they can be taken to perform lifetime calculations. Experiments, simulation, or literature study can be used to create such acceleration models. It may be that acceleration is not possible due to limiting physical boundary conditions. In such a case, minimum stress times should be defined to demonstrate sufficient robustness margin, (e.g., based on change or degradation of any electrical or physical properties during or after stress and the impact on the specific application).

**A7.3.3.2.3 Flow Chart Step 2.3: Calculate Test Duration with Selected Acceleration Models**

The acceleration model is used to calculate the acceleration factor for the standard stress condition. This in return gives the calculated minimum required stress time $t_{CALC}$ (in hrs or number of cycles) to demonstrate reliability without failures.

**A7.3.3.2.4 Flow Chart Step 2.4: Critical/Marginal Determination**

A comparison with the standard qualification duration $t_{STAND}$ is to be made. In case $t_{STAND} > t_{CALC}$, the component is assumed to be not critical/marginal. To express the robustness margin, the Robustness Indicator Figure (RIF) can be used, which is in this case defined as the ratio between $t_{CALC}$ and $t_{STAND}$ : $RIF = t_{STAND} / t_{CALC}$.

**A7.3.3.2.5 Flow Chart Step 2.5: Define Additional Tests or Provide Additional Data**

If the component standard qualification is not sufficient, the supplier may define additional tests / test conditions (as shown in Flow Chart 1) or provide/create additional data ( as shown in Flow Chart 2) via extended product qualifications, engineering studies, technology development or similar, to provide the evidence that the component is suited for the considered mission profile. With this additional data, the Robustness Indicator Figure (RIF) can be recalculated and the component may be determined to be not critical/marginal.

**A7.3.3.2.6 Flow Chart Step 2.6: Define Additional Tests or Provide Additional Data**

The possibility to create additional data (as shown in Flow Chart 1) or show that additional data is not critical/marginal determines the next step. The robustness margin can be expressed by the Robustness Indicator Figure (RIF), which is in this case defined as the ratio between the time to fail and the requested life time under use conditions (which can also be a determined minimum stress time without fail): $RIF = t_{FAIL} / t_{LIFE}$. If the RIF is below a predefined limit or even below one, it is considered critical or marginal. In the case where RIF is sufficiently high, the component is considered to be suitable.

**A7.3.3.2.7 Flow Chart 1 (Reliability Test Criteria for New Component), Result B: Perform Testing According to Mission Profile Conditions**

If the response to Flow Chart 1 step 2.6 is “Yes”, testing must be performed according to Mission Profile specific test conditions.

**A7.3.3.2.8 Flow Chart 2 (Assessment of Existing, Qualified Component), Result B: Mission Profile Validated**

If the response to Flow Chart 2 Step 2.5b is "Yes" and the Robustness Indication Factor (RIF = $t_{FAIL}$ / $t_{LIFE}$) is sufficiently high (i.e., not critical/marginal), the component is considered suitable and the Mission Profile has been validated.

**A7.3.3.3 Robustness Validation on Component Level**

If the response to step to Flow Chart 2 Step 2.5b is "No" or the Robustness Indication Factor (RIF = $t_{FAIL}$ / $t_{LIFE}$) is below a predefined limit or even below one (considered critical/marginal), Tier1 can select another component.

**A7.3.3.3.1 Flow Chart 1 (Reliability Test Criteria for New Component), Result C: Perform Robust Validation**

If the response to Flow Chart 1 Step 2.6 is "No", Robustness Validation is to be performed with detailed alignment between Tier1 and Component Manufacturer. Appropriate solutions are based on identifying the dominant load and related failure mechanism(s) and enhancing the capabilities of the existing component in an iterative manner, or improving the robustness of the system design (e.g., by redundancy, error correction), or reducing the dominant load (e.g., by improved system thermal management).

**A7.3.3.3.2 Flow Chart 2 (Assessment of Existing, Qualified Component), Result C: Perform Robust Validation**

If the response to Flow Chart 2 Step 3.1 is "No", Robustness Validation is to be performed with detailed alignment between Tier1 and Component Manufacturer. Appropriate solutions are based on identifying the dominant load and related failure mechanism(s) and enhancing the capabilities of the existing component in an iterative manner, or improving the robustness of the system design (e.g., by redundancy, error correction), or reducing the dominant load (e.g., by improved system thermal management).

## A7.4 BASIC CALCULATIONS FOR AEC-Q101 STRESS TEST CONDITIONS AND DURATIONS

According to flow chart discussed in Section A7.3, basic calculations can be made to support the decision making. The results of these calculations are based on singly-performed stress tests on given devices. More advanced methods such as sequential testing are not addressed in this section. The models and assumptions for each test are used to generate the test conditions used in this document. The user can then change the parameters used in these calculations to determine whether Robustness Validation should be used and whether a more appropriate set of test conditions should be used for the appropriate stress test.

The justification for the use of the models, constants and variables in this section can be found in JEDEC JEP122 Failure Mechanisms and Models for Semiconductor Devices.

The basic calculations in Table A7.1 for each of the major stress tests serve as an example for how one can derive suitable test conditions that address their application conditions and lifetime requirements using reasonable assumptions related to their application. Calculations using other assumptions and conditions may be just as valid for the purpose of determining the need for comprehensive Robustness Validation activities as described in Section A7.3.2.

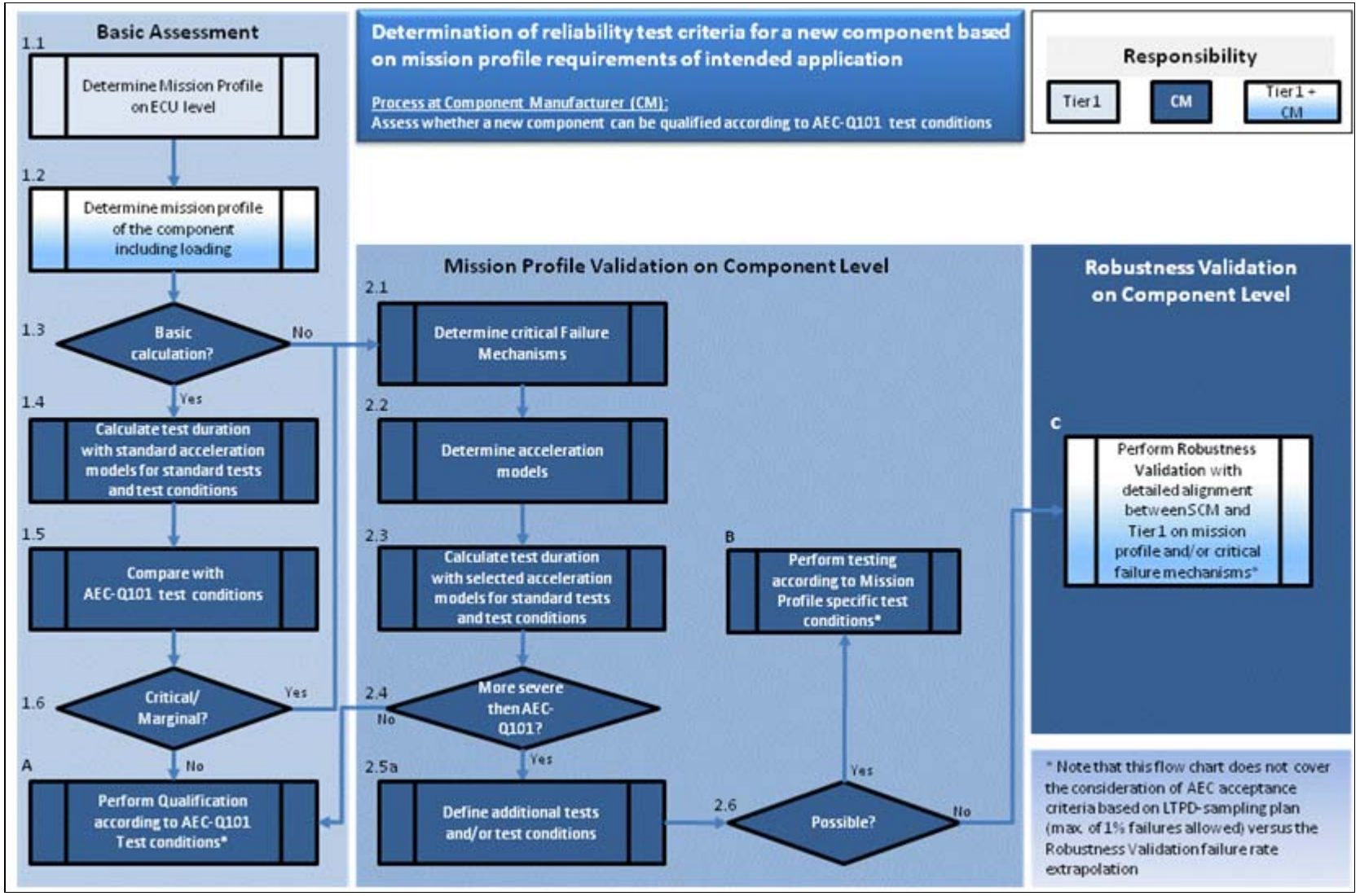


**Figure A7.1: Flow Chart 1 – Reliability Test Criteria for New Component**

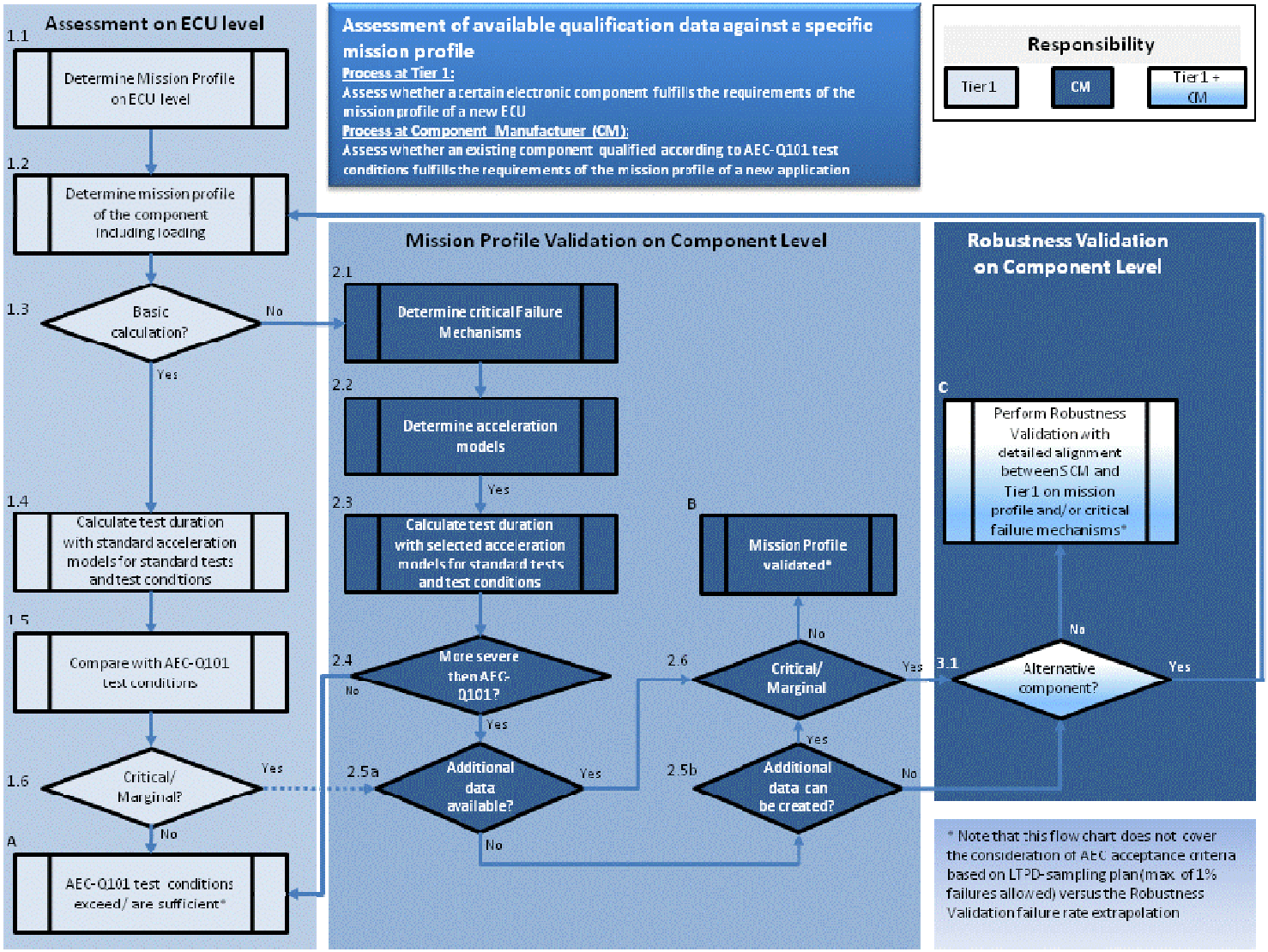


**Figure A7.2: Flow Chart 2 – Assessment of Existing, Qualified Component**

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**Component Technical Committee**

## Table A7.1: Example Calculations for AEC-Q101 Tests for Discrete Devices

| Loading | Mission Profile Input | Stress Test | Stress Conditions | Acceleration Model (All temperatures in K, not in °C) | Model Parameters | Calculated Test Duration |
|---|---|---|---|---|---|---|
| **Thermal** | Engine on:<br>$t_u$ = 12,000 hr (average engine on time over 15 yr)<br>$T_u$ = 100°C (average junction temperature in engine on mode)<br>---<br>Engine off:<br>$t_u$ = 3,000 hr (average engine off time over 15 yr)<br>$T_u$ = 55°C (average junction temperature in engine off mode) | High Temperature Reverse Bias (HTRB)<br>or<br>High Temperature Gate Bias (HTGB) | $T_t$ = 150°C (junction temperature in test environment) | Arrhenius<br>$A_f = \exp\left[\frac{E_a}{k_B} \bullet \left(\frac{1}{T_u} - \frac{1}{T_t}\right)\right]$<br>Also applicable for High Temperature Storage | $E_a$ = 0.7 eV<br>(activation energy; 0.7 eV is a typical value, actual values depend on failure mechanism and range from -0.2 to 1.4 eV)<br>$k_B$ = 8.61733 x $10^{-5}$ eV/K<br>(Boltzmann's Constant) | $t_t$ = 916 hr (test time)<br>$t_t = \frac{t_u}{A_f}$<br>---<br>$t_t$ = 12 hr (test time)<br>$t_t = \frac{t_u}{A_f}$ |
| | | | | | **Total Test Time:** | $t_t$ = 928 hr |
| **Thermo-Mechanical** | $n_u$ = 54,750 cls (number of engine on/off cycles in 15 yr)<br>$\Delta T_u$ =70°C (average thermal cycle temperature change in use environment:<br>$T_u$ @ engine on 100°C<br>$T_u$ @ engine off 30°C) | Temperature Cycling (TC) | $\Delta T_t$ =205°C (thermal cycle temperature change in test environment:<br>-55°C to 150°C) | Coffin Manson<br>$A_f = \left(\frac{\Delta T_t}{\Delta T_u}\right)^m$ | m = 4<br>(Coffin Manson exponent; 4 is to be used for cracks in hard metal alloys, actual values depend on failure mechanisms and range from 1 for ductile to 9 for brittle materials) | $n_t$ =744 cls (number of cycles in test)<br>$n_t = \frac{n_u}{A_f}$ |
| | $n_u$ = 54,750 cls (number of engine on/off cycles in 15 yr)<br>$\Delta T_u$ =55°C (average thermal cycle temperature change in use environment:<br>$T_u$ @ engine on 125°C<br>$T_u$ @ engine off 70°C) | Intermittent Operating Life (IOL)<br>&<br>Power Temperature Cycling (PTC) | $\Delta T_t$ =100°C (thermal cycle temperature change in test environment:<br>25°C to 125°C) | Coffin Manson<br>$A_f = \left(\frac{\Delta T_t}{\Delta T_u}\right)^m$ | m = 2.5<br>(Coffin Manson exponent; 2.5 is to be used for die bond solder joint fatigue, actual values depend on failure mechanisms and range from 1 for ductile to for brittle materials) | $n_t$ =12,283 cls (number of cycles in test)<br>$n_t = \frac{n_u}{A_f}$ |

## Table A7.1: Example Calculations for AEC-Q101 Tests for Discrete Devices (continued)

| Loading | Mission Profile Input | Stress Test | Stress Conditions | Acceleration Model (All temperatures in K, not in °C) | Model Parameters | Calculated Test Duration |
|---|---|---|---|---|---|---|
| Humidity | Engine on:<br>$t_u$ = 12,000 hr (average engine on time over 15 yr)<br><br>$RH_u$ = 20% (average relative humidity in on mode)<br><br>$T_u$ = 100°C (average junction temperature in engine on mode) | High Humidity High Temperature Reverse Bias ($H^3TRB$)<br><br>&<br><br>Highly Accelerated Stress Test (HAST) | $RH_t$ = 85% (relative humidity in test environment)<br><br>$T_t$ = 85°C for $H^3TRB$<br>$T_t$ = 110°C for HAST/110<br>$T_t$ = 130°C for HAST/130 (ambient temperature in test environment) | Hallberg-Peck<br>$A_f = \left(\frac{RH_t}{RH_u}\right)^p \bullet \exp\left[\frac{E_a}{k_B} \bullet \left(\frac{1}{T_u} - \frac{1}{T_t}\right)\right]$<br>(See Notes below) | p = 3<br>(Peck exponent, 3 is to be used for bond pad corrosion)<br><br>$E_a$ = 0.9 eV<br>(activation energy; 0.9 eV)<br><br>$k_B$ = 8.61733 x $10^{-5}$ eV/K<br>(Boltzmann's Constant) | $t_t$ = 505 hr ($H^3TRB$)<br>$t_t$ = 75 hr (HAST/110)<br>$t_t$ = 19 hr (HAST/130)<br>(test time)<br>$t_t = \frac{t_u}{A_f}$ |
| | Engine off:<br>$t_u$ = 3,000 hr (average engine off time over 15 yr)<br><br>$RH_u$ = 60% (average relative humidity in off mode)<br><br>$T_u$ = 55°C (average junction temperature in engine off mode) | | $RH_t$ = 85% (relative humidity in test environment)<br><br>$T_t$ = 85°C for $H^3TRB$<br>$T_t$ = 110°C for HAST/110<br>$T_t$ = 130°C for HAST/130 (ambient temperature in test environment) | | | $t_t$ = 73 hr ($H^3TRB$)<br>$t_t$ = 11 hr (HAST/110)<br>$t_t$ = 3 hr (HAST/130)<br>(test time)<br>$t_t = \frac{t_u}{A_f}$ |
| | Engine Non-operating:<br>$t_u$ = 116,400 hr (average engine off time over 15 yr)<br><br>$RH_u$ = 75% (average relative humidity in off mode)<br><br>$T_u$ = 30°C (average junction temperature in engine off mode) | | $RH_t$ = 85% (relative humidity in test environment)<br><br>$T_t$ = 85°C for $H^3TRB$<br>$T_t$ = 110°C for HAST/110<br>$T_t$ = 130°C for HAST/130 (ambient temperature in test environment) | | | $t_t$ = 402 hr ($H^3TRB$)<br>$t_t$ = 60 hr (HAST/110)<br>$t_t$ = 16 hr (HAST/130)<br>(test time)<br>$t_t = \frac{t_u}{A_f}$ |
| | | | | | **Total Test Time:** | $t_t$ = 980 hr ($H^3TRB$)<br>$t_t$ = 146 hr (HAST/110)<br>$t_t$ = 38 hr (HAST/130) |

Note 1: Autoclave (121°C / 100% RH) is a highly accelerated test using a saturated moisture condition that will tend to uncover failure mechanisms not seen in normal use conditions. For this reason, autoclave is not a test whose test conditions can be derived through models and assumptions. The current test conditions were selected decades ago and the test has been used as part of a standard qualification ever since.

Note 2: Most Pressure Pot testing is performed with an Al Pressure Pot. Air purging is done at 100°C boiling water, and with both steam and liquid escaping from the vent. The chamber walls are not independently heated at all. Control of the chamber wall temperature; air purging procedure, during ramp-up; ramp-down temperature and pressure and overall temperature and pressure are key. In addition, when the test is ended the heater is turned off and the vent is opened. It takes about 3 minutes to fully vent the pot. A significant concern is that venting before the pot chamber drops to 100°C, can cause a pressure differential from the >100°C residual hot device and cause any water trapped in device void to create a pop-corning type of delamination.

# Revision History

| Rev # | Date of change | Brief summary listing affected sections |
|---|---|---|
| - | May 15, 1996 | Initial Release |
| A | May 5, 1999 | General Revision - Corrected errors, made clarifications, changed lot requirements. Removed CDF and “Automotive Grade” designations throughout. |
| B | July 25, 2000 | Update signature block on page 1; Removed "Parts must be mounted to test boards." from "Additional Requirements" for Pre-conditioning in Table 1 page 8; Changed "IOL" to "PTC" in "Additional Requirements" for Power and Temperature Cycle in Table 1 page 9; Removed revision from "Reference" for Resistance to Solder Heat in Table 1 page 10 (i.e. B-106-A becomes B-106); Added note U to "Legend for Tables 1 and 2" on page 11. |
| C | June 29, 2005 | Revised table numbers throughout document<br>Section 1.1.2 - Definition of Stress Test Qualification clarification<br>Section 1.2.2 – Delete one, add two Industrial standard references<br>Section 1.2.3 – Delete two, add one AEC standard references<br>Section 1.2.4 – Add two quality standard references<br>Section 2.1 – Define what "AEC Q101 Qualified" means<br>Section 2.3 – Reference to Table 1<br>Table 1 – Part Qualification/Requalification Lot Requirements<br>Section 2.4.3 - Editorial<br>Section 2.5 – Current leakage measurement accuracy limit<br>Section 3.2 – Requirements of supplier for process changes<br>Section 3.2.1 – Process Change definition<br>Section 3.2.2 – Remove reference<br>Section 4.2 – Family data disallowance clarification<br>Section 4.3 – Charged Device Model limitations<br>Section 4.4 – Reference to TS-16949<br>Table 2: Qualification Test Definitions<br>Test 2 – PC before PTC required<br>Test 3 – JEDEC reference<br>Test 5 – Ambient/Junction temperature requirements<br>Test 6 - Ambient/Junction temperature requirements<br>Test 7 – Temperature extremes requirement<br>Test 8 – Added note<br>Test 9 – Ambient temperature and test requirements<br>Test 9alt – New alternative test option<br>Test 10 – Test requirement and added note<br>Test 10alt – Test criteria, requirement and added note<br>Test 11 – Criteria for CDM requirement<br>Test 12 – HAST as alternative<br>Test 20 – Allowance for alteration of test method<br>Test 21 – Clarification of test method<br>Legend – 5 new notes to table 2<br>Table 2A – IOL/PTC cycling requirements per package type<br>Table 2B – Solder conditions per package type<br>Table 3 – New changes and notes added |

| Rev # | Date of change | Brief summary listing affected sections |
|---|---|---|
| C (cont.) | | Appendix 2 – Reference to website, clarify requirements<br>Appendix 3 – Reference to website<br>Appendix 4 - Reference to website |
| D | May 18, 2013 | Complete Revision. Revised document title to reflect that the stress test qualification requirements are failure mechanism based. Revised Sections 1.2., 1.2.3, 2.2, 2.3, 2.4.4, 2.5, 2.6, 2.7, 3.1, 3.2, 3.2.1 to 3.2.4, 4.3, Appendix 1, Appendix 2, Appendix 4, Figure A4.1, and Tables 1 to 3. Added Sections 1.2.5, 1.3, 1.3.1 to 1.3.3, 2.4.5, 4.5, Appendix 6, Appendix 7, Figures 1, A7.1, A7.2, and Tables 2A, 2B, A7.1. Deleted Sections 1.1.2, 1.1.3, and 2.1. |